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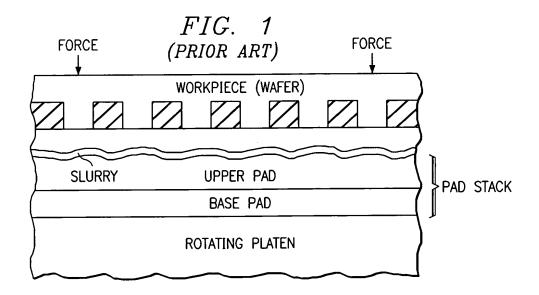
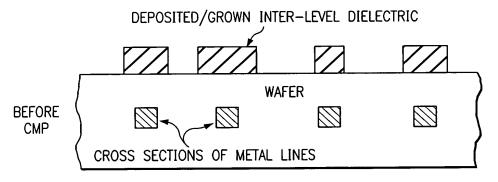
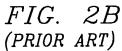
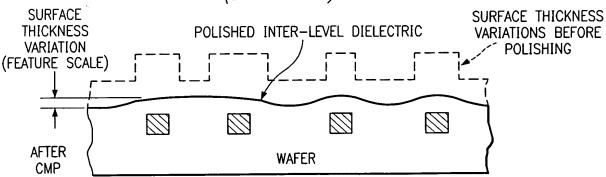


FIG. 2A (PRIOR ART)







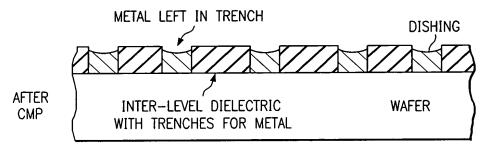
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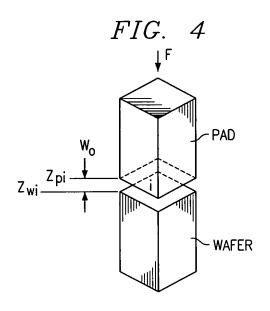
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FIG. 3A (PRIOR ART)

BEFORE CMP INTER-LEVEL DIELECTRIC WITH TRENCHES FOR METAL WAFER

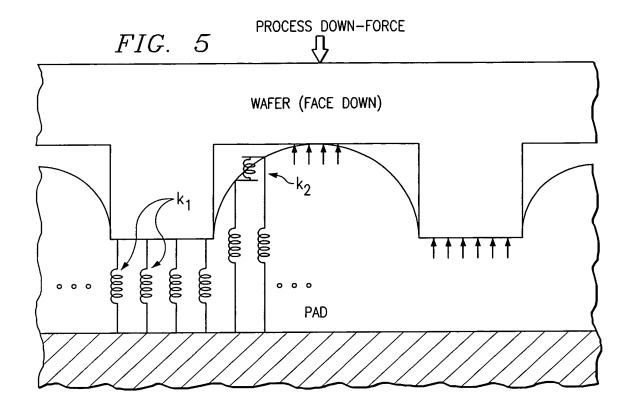
FIG. 3B (PRIOR ART)

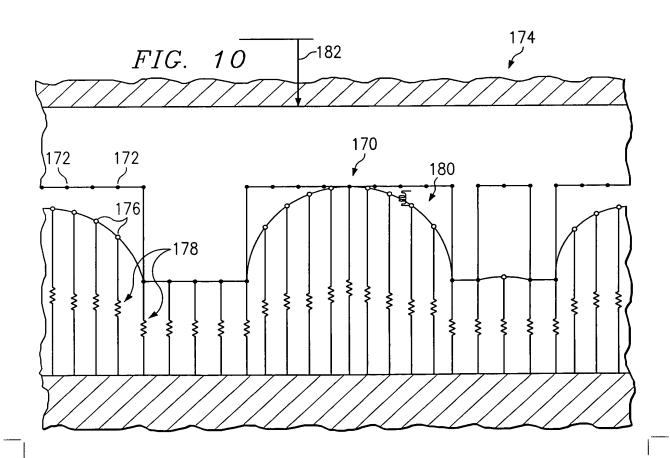




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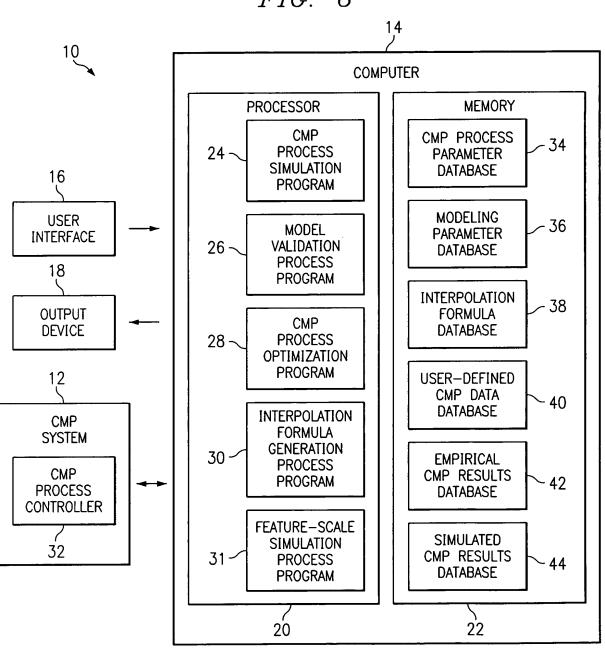
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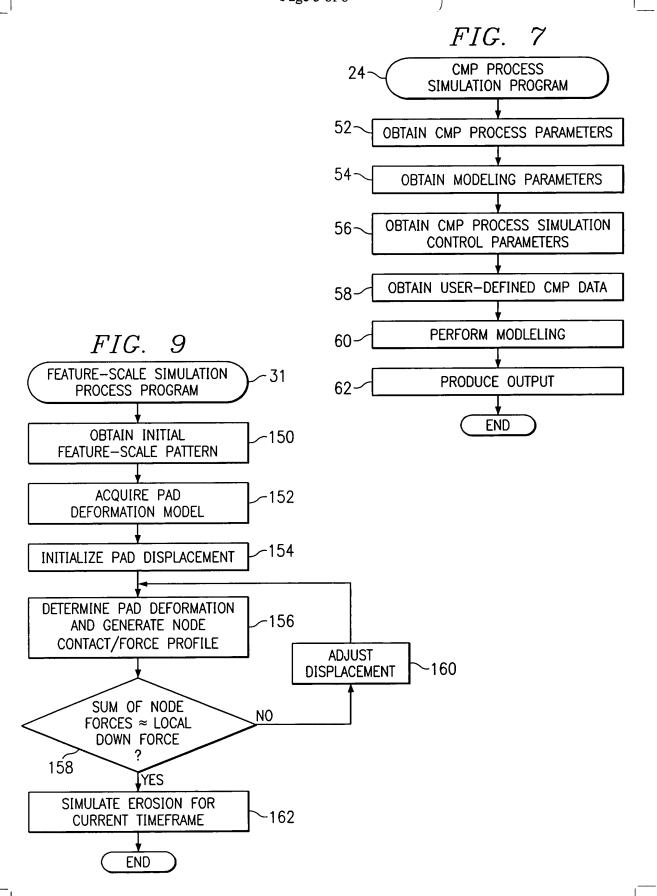


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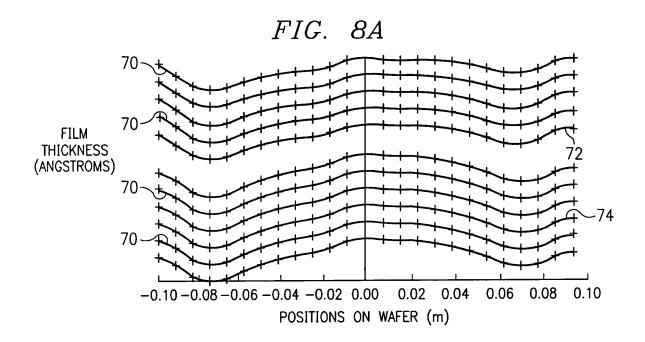
FIG. 6

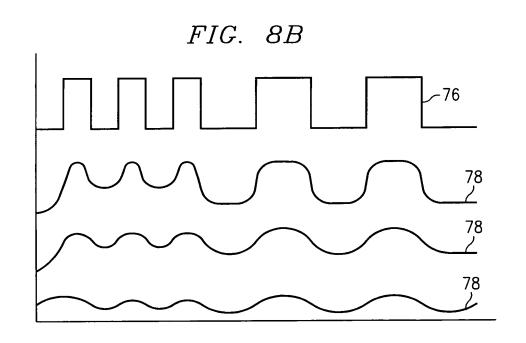


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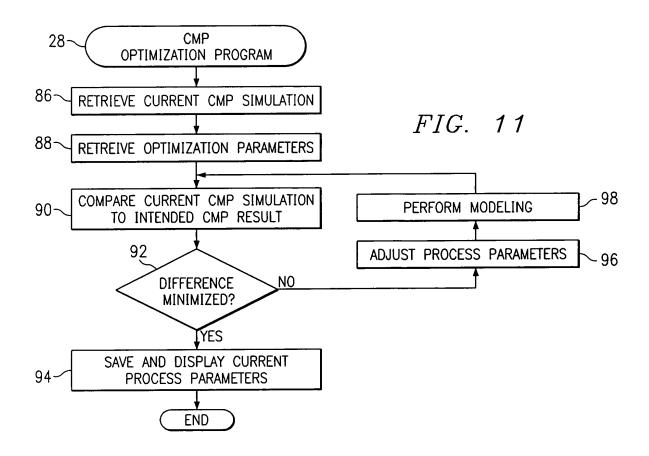


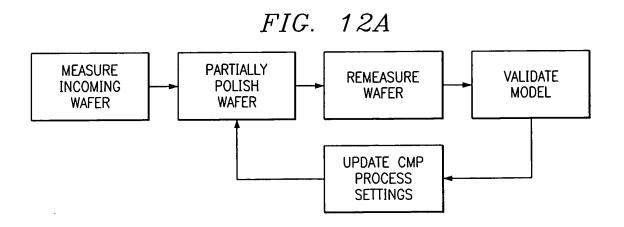
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